UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,530	03/29/2004	Volker Harle	12406-140001	5329

26161 7590 12/22/2008
FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
12/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/813,530	HARLE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-34* is/are allowed.

6)☒ Claim(s) *1,2,6,7,12-14 and 22-25* is/are rejected.

7)☒ Claim(s) *5,8-11 and 15-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/11/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Examiner Amendment.*.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

AUTHORIZATION

Authorization for this examiner's amendment was given in a telephone interview with Mr. Marc Wefer on November 26, 2008.

TO CLAIMS

To add claim 4 into the independent claim 1 and cancel the claim 4.

Therefore, the claim 1:

(1) A method for fabricating a semiconductor component, which comprises the steps of:

providing a semiconductor body containing a substrate (160) and at least one nitride compound semiconductor disposed on the substrate (160) (see Figure 10);

applying a metal layer to a surface of the semiconductor body (see Figure 10); dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer, previously covered by the removed metal layer, wherein the dry-chemically removing is performed by forming a mask on the metal layer, a part of the metal layer not being covered by the mask, removing that part of the metal layer which is not covered by the mask, a part of the surface of the

semiconductor body thereby being uncovered and defining an uncovered surface, partially removing the semiconductor body in regions of the uncovered surface, and removing the mask, which further comprises forming the mask as a dielectric mask which contains at least one material selected from the group consisting of silicon oxide, aluminum oxide, silicon nitride, titanium oxide, Ta oxide, zirconium oxide, and a layer system containing at least one of the materials.

Response to Arguments

Applicant's arguments with respect to claims 1-2 and 5-34 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1, 7, 12, 14 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (U.S. 6,083,841) in view of Frank (U.S. 5,277,750).

Yano discloses a GaN-based compound semiconductor layer with

(1) providing a semiconductor body (1, 2) containing a substrate (1) and at least one nitride compound semiconductor (2) disposed on the substrate (1) (see Figure 1a);

applying a metal layer (3) to a surface of the semiconductor body (1, 2) (see Figure 1a);

dry-chemically removing a part of the metal layer (3) and a part of the semiconductor body (1, 2) previously covered by the removed metal layer (3), previously covered by the removed metal layer (3), wherein the dry-chemically removing is performed by forming a mask (4) on the metal layer (3), a part of the metal layer (3) not being covered by the mask (4), removing that part of the metal layer (3) which is not covered by the mask (4), a part of the surface of the semiconductor body (1, 2) thereby being uncovered and defining an uncovered surface, partially removing the semiconductor body (1, 2) in regions of the uncovered surface, and removing the mask (4) (see Figures 1(a) through 1(c));

(7) which further comprises removing the part of the semiconductor body by an etching method (see column 5, lines 21-34);

(12) which further comprises applying a contact metallization (see Figure 2);

(25) which further comprises removing the metal layer by an etching method (see column 5, lines 21-34).

Yano teaches everything above except for which further comprises forming the mask as a dielectric mask which contains at least one material selected from the group consisting of silicon oxide, silicon nitride, and a layer system containing at least one of

the materials and the thickness of the metal layer. However, Frank discloses an integrated semiconductor circuit with **(1)....** which further comprises forming the mask (4) as a dielectric mask which contains at least one material selected from the group consisting of silicon oxide, silicon nitride and a layer system containing at least one of the materials (see column 5, lines 55-60). Even through, Yano and Frank do not explicitly describe the thickness of the metal layer. However, the thickness of the metal layer is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Yano (accordance with the teaching of Frank) since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice, and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Leshin, 125 USPQ 416 and In re Aller, 105 USPQ 233 (see MPEP 2144.05). Additionally, since Yano and Frank are both from the same field of endeavor (semiconductors), the purpose disclosed by Frank would have been recognized in the pertinent art of Yano.

Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (U.S. 6,083,841) in view of Frank (U.S. 5,277,750) and further in view of Cervantes et al. (U.S. 6,379,985).

Yano and Frank teach the above outlined features with the exception of selecting the nitride compound semiconductor as a compound having a formula $Al_yIn_xGa_{1-x-y}N$, $0<x<1$, $0<y<1$, $0<x+y<1$. Furthermore, Cervantes discloses a semiconductor device with **(2)** which further comprises forming the nitride compound semiconductor as a compound having a formula $Al_yIn_xGa_{1-x-y}N$, $0<x<1$, $0<y<1$, $0<x+y<1$ (see column 11, line 3); **(13)** which further comprises forming the metal layer to contain a material selected from the group consisting of platinum and palladium (see column 9, lines 35-38). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Yano and Frank (accordance with the teaching of Cervantes) since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Additionally, since Yano, Frank and Cervantes are from the same field of endeavor (semiconductors), the purpose disclosed by Cervantes would have been recognized in the pertinent art of Yano and Frank.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (U.S. 6,083,841) in view of Frank (U.S. 5,277,750) and further in view of Losehand et al. (U.S. 6,448,162).

Yano and Frank teach everything above except for removing the metal layer by a sputtering-back method. Furthermore, Losehand discloses a Schottky diode with **(6)** which further comprises removing the metal layer by a sputtering-back method (see

column 4, line 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Yano and Frank (accordance with the teaching of Losehand) since the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight and also it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Additionally, since Yano, Frank and Losehand are from the same field of endeavor (semiconductors), the purpose disclosed by Losehand would have been recognized in the pertinent art of Yano and Frank.

Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano et al. (U.S. 6,083,841) in view of Frank (U.S. 5,277,750) and Cervantes et al. (U.S. 6,379,985) and further in view of Losehand et al. (U.S. 6,448,162).

Yano and Frank teach the above outlined features with the exception of selecting which further comprises forming the substrate to be n-conducting; which further comprises forming the substrate to be selected from the group consisting of n-doped SiC and n-doped GaN. However, Cervantes discloses a semiconductor device with **(23)** which further comprises forming the substrate to be selected from the group consisting of n-doped GaN (see column 9, lines 23-25). Furthermore, Losehand discloses a Schottky diode with **(22)** which further comprises forming the substrate to be n-conducting (see column 3, lines 19-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

teachings of Yano, Frank and Cervantes (accordance with the teaching of Losehand) since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Additionally, since Yano, Frank, Cervantes and Losehand are from the same field of endeavor (semiconductors), the purpose disclosed by Losehand would have been recognized in the pertinent art of Yano, Frank and Cervantes.

Allowable Subject Matter

Claims 5, 8-11, 15-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 26-34 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined claims define over the prior art. The cited prior art does not disclose or suggest a semiconductor device inter alia the limitations ". .... applying a passivation layer to the surface of the semiconductor body and part of the metal layer, at least a further part of the metal layer not being covered by the passivation layer, wherein applying the passivation layer comprises applying the passivation layer as a continuous passivation layer to the surface of the semiconductor body and the part of the metal

layer, applying a mask on the continuous passivation layer, the mask not covering the passivation layer at least in a region in which the passivation layer adjoins the metal layer, removing parts of the passivation layer which are not covered with the mask, and removing the mask. ..."

.Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
December 10, 2008